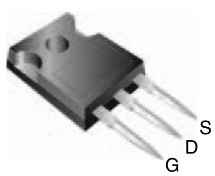
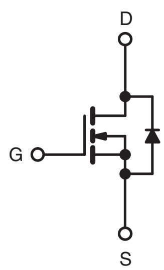
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.060
Q_g (Max.) (nC)	210	
Q_{gs} (nC)	34	
Q_{gd} (nC)	94	
Configuration	Single	

TO-247





N-Channel MOSFET

FEATURES

- Advanced Process Technology
- Dynamic dV/dt Rating
- 175 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Available

RoHS*
COMPLIANT

DESCRIPTION

Fifth generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well know for, provides the designer with an ectremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP264NPbF
	SiHFP264N-E3
SnPb	IRFP264N
	SiHFP264N

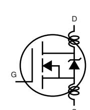
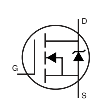
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	250	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	44	A
		T_C = 100 °C		31	
Pulsed Drain Current[a]			I_{DM}	170	
Linear Derating Factor				2.6	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	520	mJ
Repetitive Avalanche Current[a]			I_{AR}	25	A
Repetitive Avalanche Energy[a]			E_{AR}	38	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	380	W
Peak Diode Recovery dV/dt[c]			dV/dt	8.7	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 1.7 mH, R_G = 25 Ω, I_{AS} = 25 A, V_{GS} = 10 V (see fig. 12).
c. $I_{SD} \le 25$ A, dI/dt ≤ 500 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 175$ °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.39	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	250	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.30	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 25 A[b]	-	-	0.060	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 25 A[b]	29	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	3860	-	pF
Output Capacitance	C_{oss}		-	480	-	
Reverse Transfer Capacitance	C_{rss}		-	110	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 25 A, V_{DS} = 200 V, see fig. 6 and 13	-	-	210	nC
Gate-Source Charge	Q_{gs}		-	-	34	
Gate-Drain Charge	Q_{gd}		-	-	94	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 25 A , R_G = 1.8 Ω, V_{GS} = 10 V, see fig. 10[b]	-	17	-	ns
Rise Time	t_r		-	62	-	
Turn-Off Delay Time	$t_{d(off)}$		-	52	-	
Fall Time	t_f		-	53	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	5.0	-	nH
Internal Source Inductance	L_S		-	13	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	44	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	170	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 25 A, V_{GS} = 0 V[b]	-	-	1.3	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 25 A, dI/dt = 100 A/µs[b]	-	270	400	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.7	4.1	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

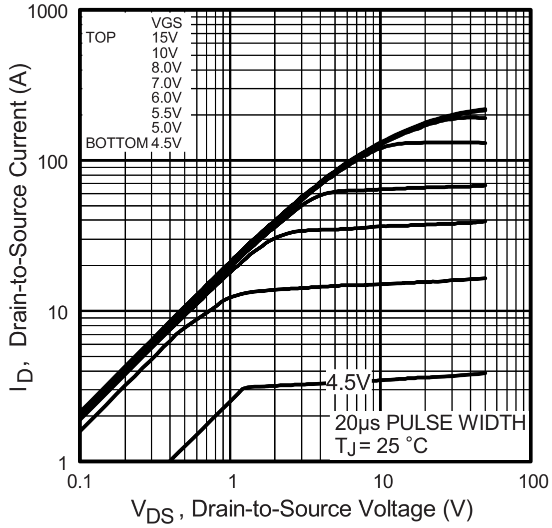


Fig. 1 - Typical Output Characteristics

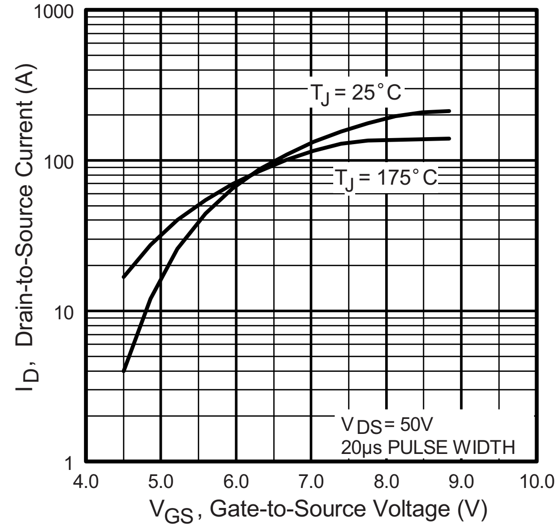


Fig. 3 - Typical Transfer Characteristics

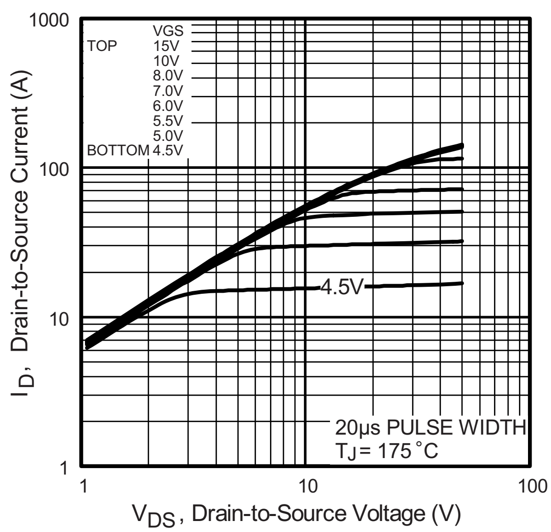


Fig. 2 - Typical Output Characteristics

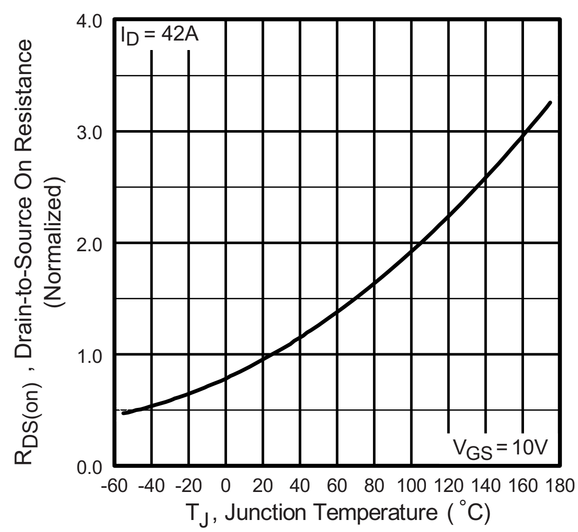


Fig. 4 - Normalized On-Resistance vs. Temperature

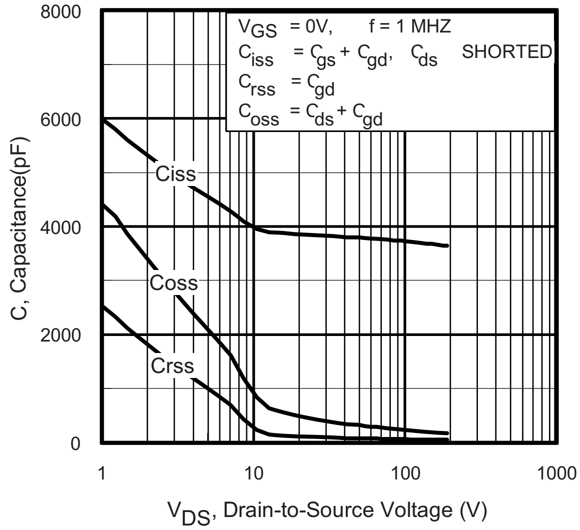


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

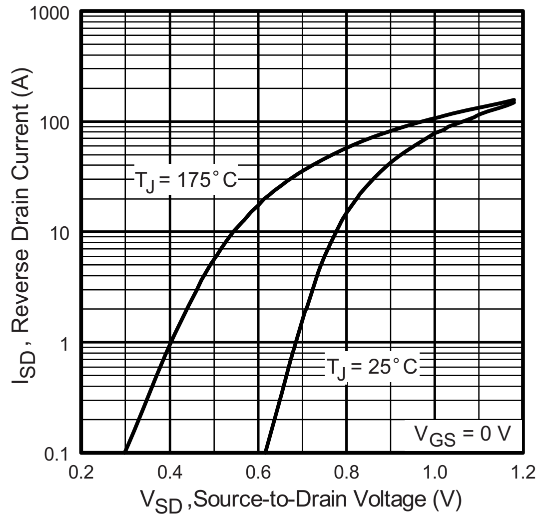


Fig. 7 - Typical Source-Drain Diode Forward Voltage

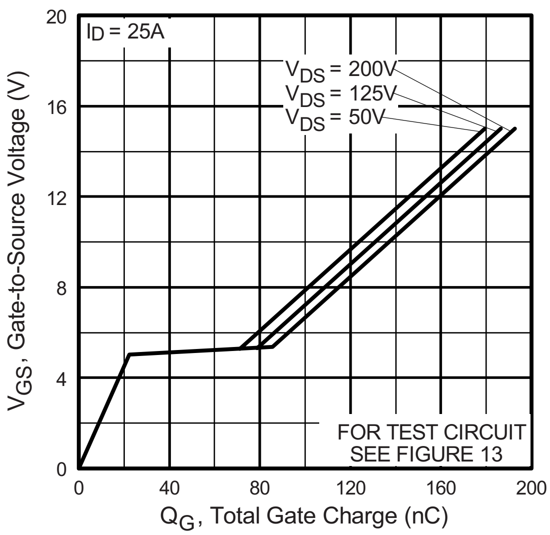


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

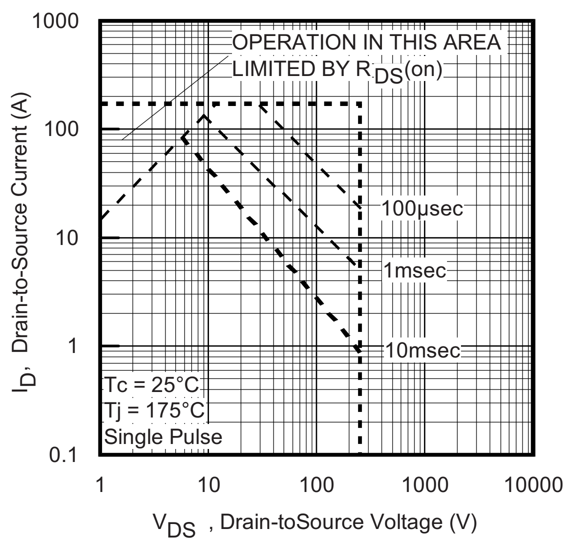


Fig. 8 - Maximum Safe Operating Area

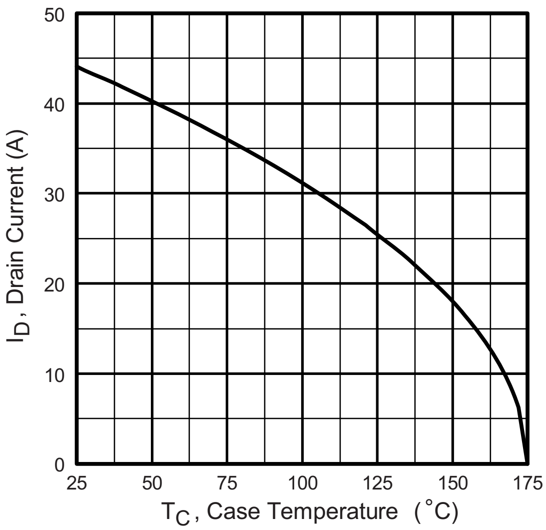


Fig. 9 - Maximum Drain Current vs. Case Temperature

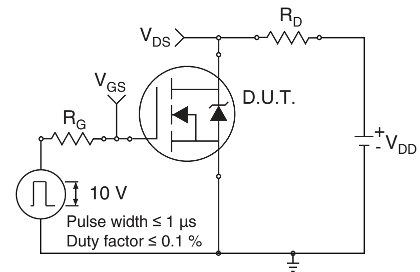


Fig. 10a - Switching Time Test Circuit

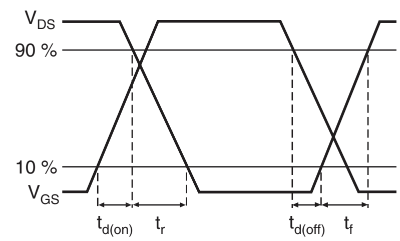


Fig. 10b - Switching Time Waveforms

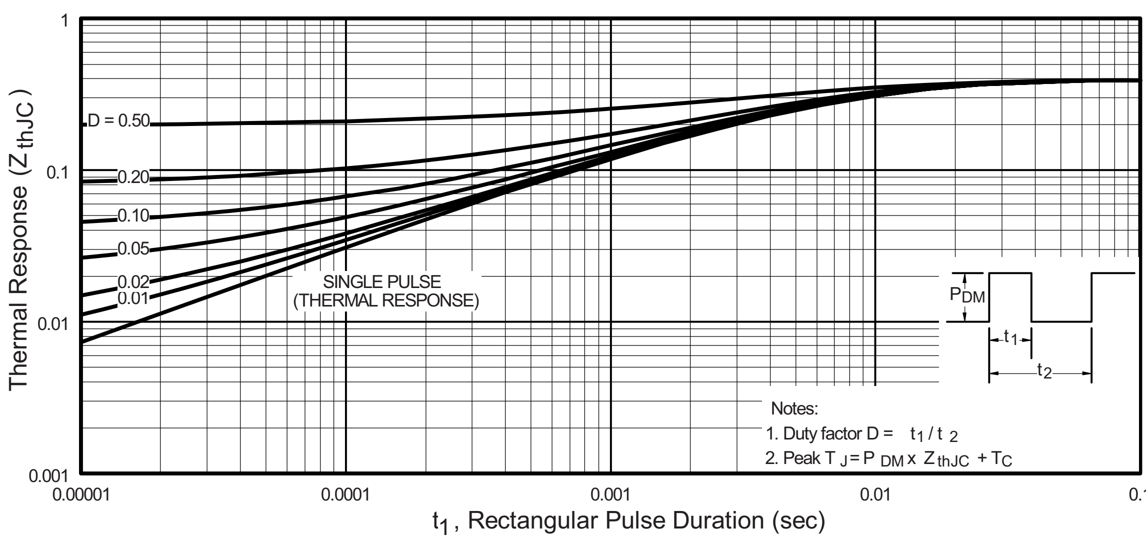


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

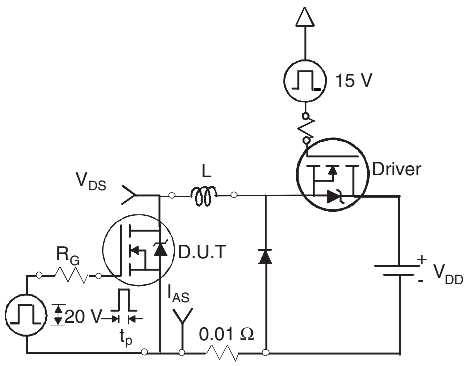


Fig. 12a - Unclamped Inductive Test Circuit

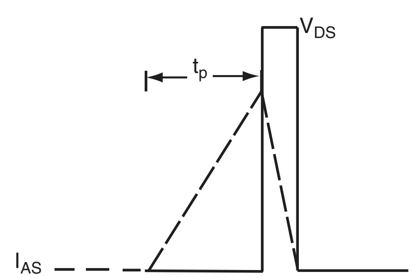


Fig. 12b - Unclamped Inductive Waveforms

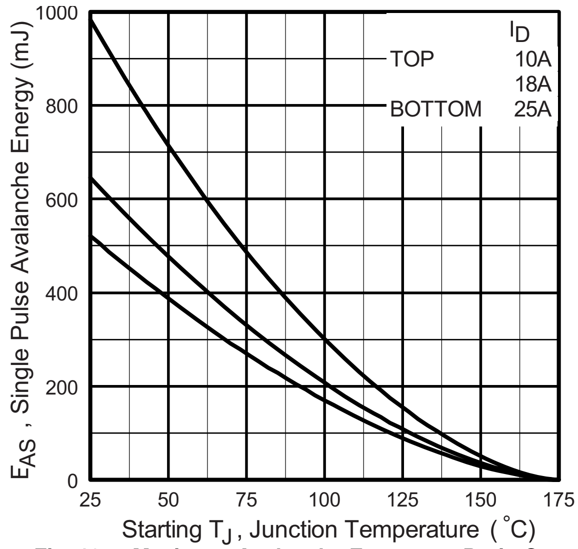


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

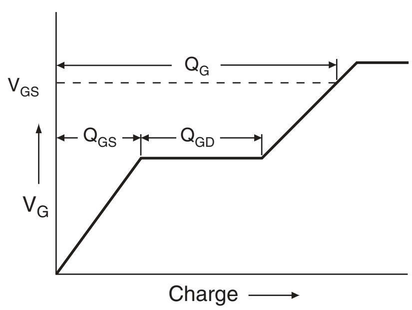


Fig. 13a - Basic Gate Charge Waveform

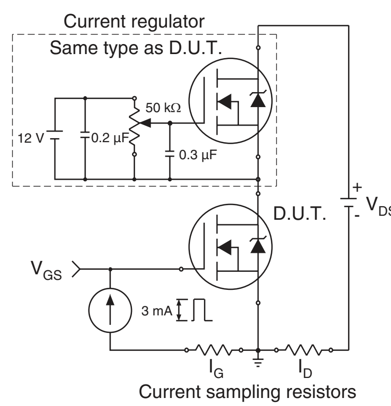
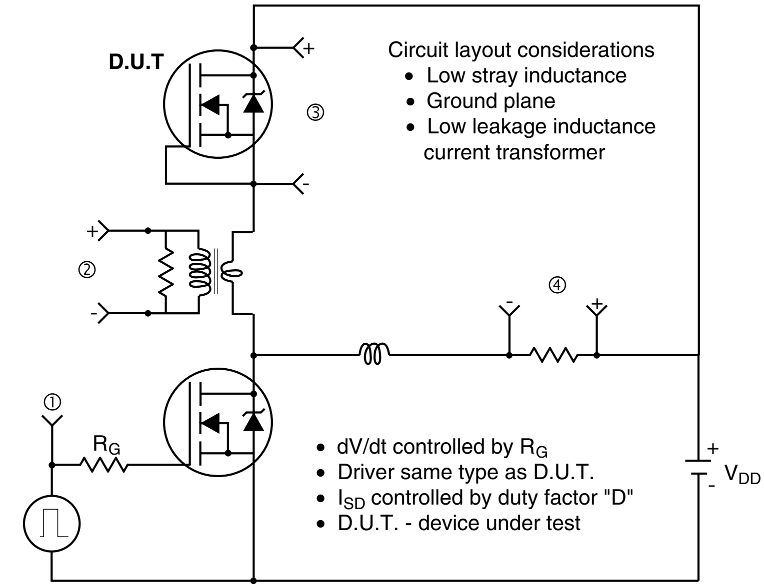
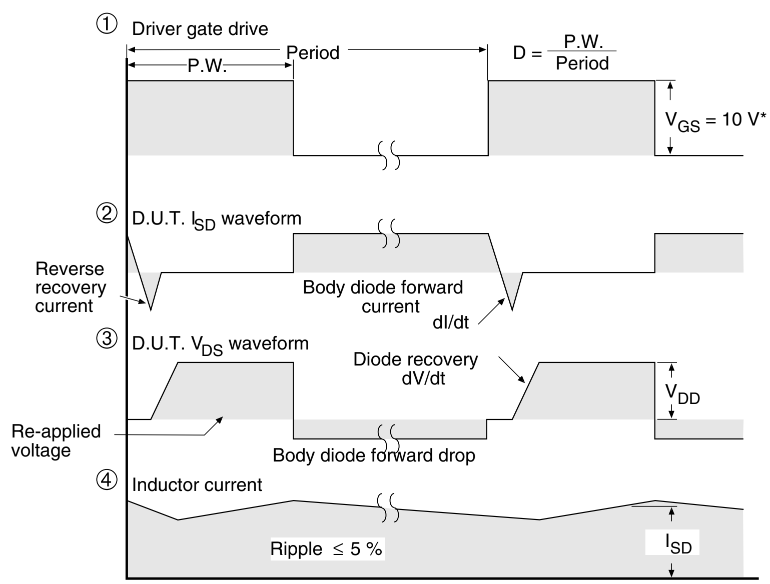


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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